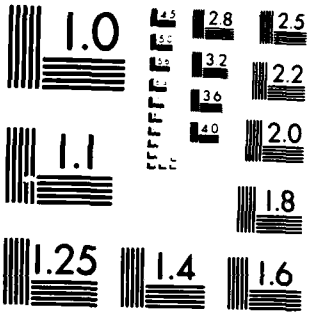
AD-A122 324 NEW NONVOLATILE MEMORY WITH RAM CAPABILITIES AND INTRINSIC RADIATION HARDNESS(U) HARRY DIAMOND LABS ADELPHI MD P S BRODY ET AL. OCT 82 HDL-TM-82-14 1/1

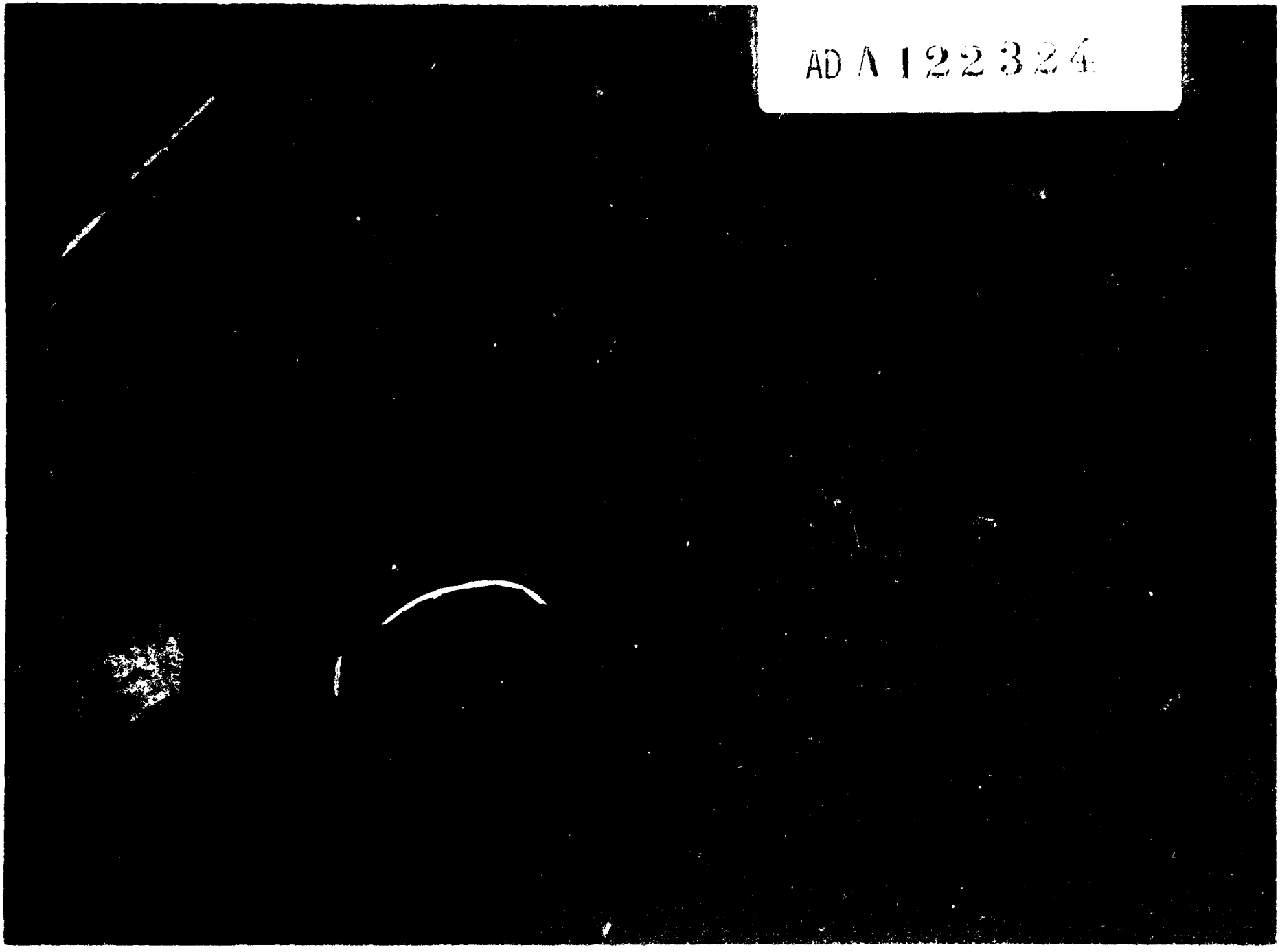
UNCLASSIFIED F/G 9/1 NL

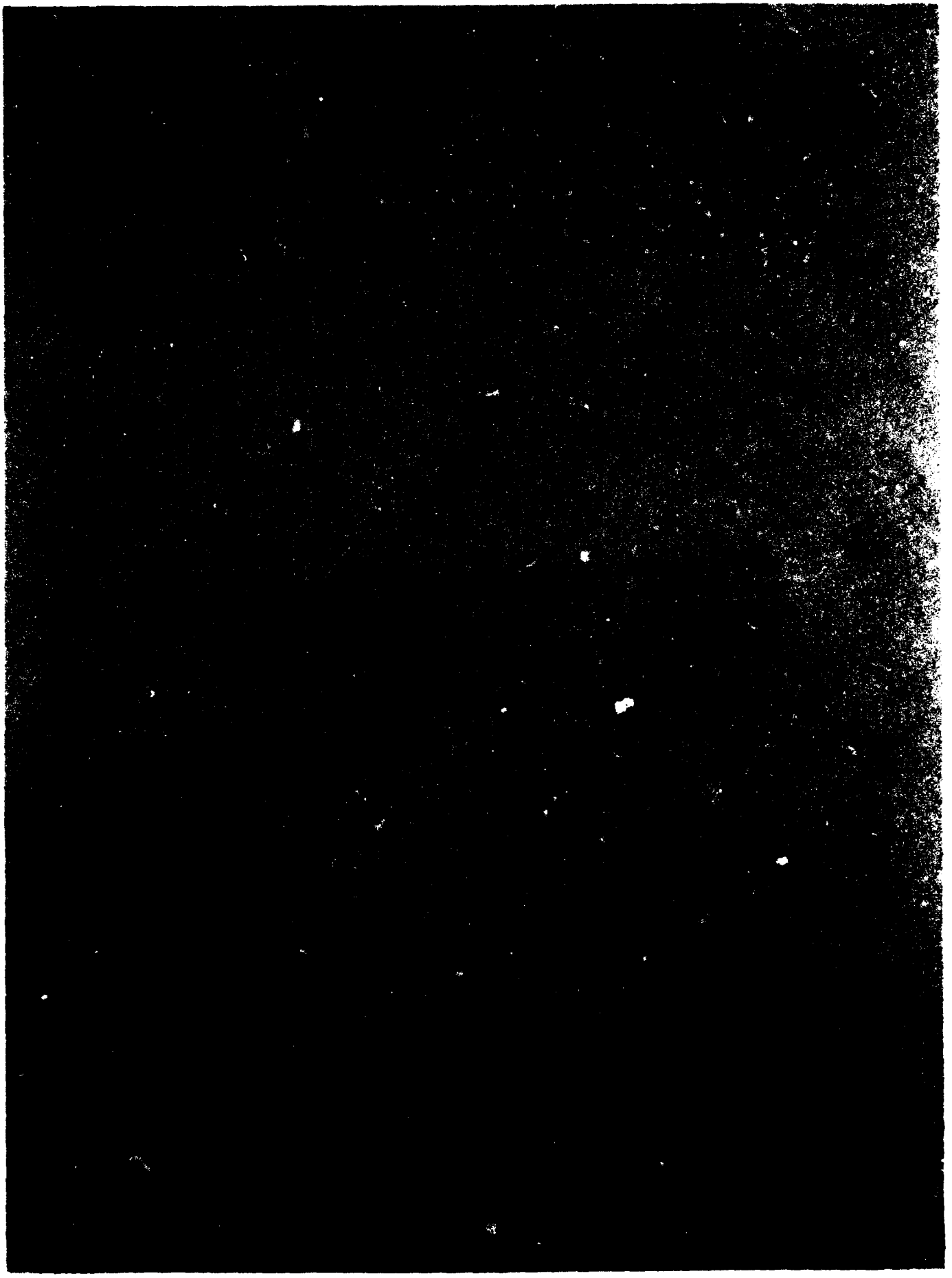
END

DATE FILMED

DTIC







UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER HDL-TM-82-14	2. GOVT ACCESSION NO. AD-A122324	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) New Nonvolatile Memory with RAM Capabilities and Intrinsic Radiation Hardness		5. TYPE OF REPORT & PERIOD COVERED Technical Memorandum 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Philip S. Brody Emanuel Katzen		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Harry Diamond Laboratories 2800 Powder Mill Rd Adelphi, MD 20783		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Program Ele: 6.21.20.A
11. CONTROLLING OFFICE NAME AND ADDRESS U.S. Army Materiel Development and Readiness Command 5001 Eisenhower Ave Alexandria, VA 22333		12. REPORT DATE October 1982 13. NUMBER OF PAGES 28
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

HDL Project: A102C4 DA Project: 1L161101A91A
DRCMS Code: 61110191A0011 PRON: 1F2R0007011FA9

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Digital memory
Photovoltaic

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The theory and performance are presented for a new type of semiconductor EAPROM (electronically alterable, programmable, read-only memory) cell using ferroelectric elements. The memory is capable of high-speed RAM operation. Experiments show that the intrinsic memory states are hard to total γ dose and to $\dot{\gamma}$.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

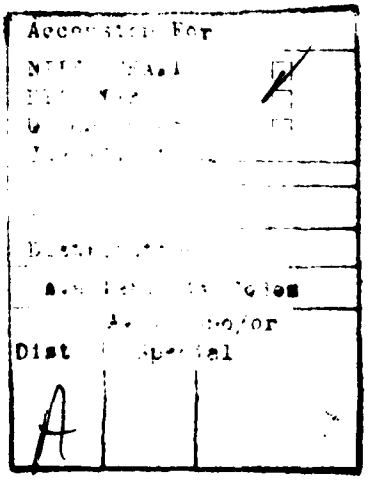
UNCLASSIFIED

CONTENTS

FIGURES

FIGURES (Cont'd)

TABLE



1. INTRODUCTION

This report describes theoretical and experimental work performed in connection with the development of a new kind of electronic computer memory. The memory is based on a hybrid combination of semiconductor and ferroelectric ceramic elements which uses an anomalous photovoltaic effect[1-4] found in the ferroelectric ceramics. This memory is a variation on the conventional static or dynamic semiconductor memories in common use. Conventional devices are volatile memories which lose their information content when power to the devices is interrupted. Devices based on the new concept, however, are nonvolatile. In some respects they have memory characteristics similar to those of metal nitride oxide semiconductor (MNOS) and floating gate EAPROM (electrically alterable programmable read-only memory) devices. The new photovoltaic ferroelectric-semiconductor, however, can be expected to be superior to the presently available EAPROM devices. This new device will excel in programming time, in the number of possible read/write cycles, and in retention of the encoded memory states. Based on the work described in this report, the device is also expected to be superior in surviving environmental radiation.

The digital photovoltaic-ferroelectric-semiconductor memory cell concept has been described and demonstrated.[5,6] Within a semiconductor read/write cell there is incorporated an additional element which is a photovoltaic ferroelectric ceramic element. In operation, this element always retains, within its molecular structure, the last written bit in the memory state. The state characteristic is one of two directions of remanent polarization. This polarization is encoded by a write pulse with an addressing transistor at the same time that a sense transistor is encoded with a gate charge. The same addressing transistor places a volatile charge (positive or negative) on the gate of the sense transistor gate and encodes the ferroelectric element, switching the remanent polarization if the memory state is to be changed. The encoded ferroelectric elements are then used at any time to place a charge on the gates of the sense transistor, even after the original gate charge has leaked off. To charge the sense transistor gates and to maintain a charge requires that the encoded ferroelectric elements be illuminated.

---

[1] *P. S. Brody, Solid State Comm. 12 (1973), 673.*

[2] *P. S. Brody, J. Solid State Chemistry 12 (1975), 673.*

[3] *For a recent review, see R. Von Baltz, Bulk Photovoltaic Effect in Ferro- and Piezoelectric Materials, Ferroelectrics, 35 (1981), 131.*

[4] *P. S. Brody, Ferroelectrics 38 (1981), 939.*

[5] *P. S. Brody, Appl. Phys. Lett. 38 (February 1981), 673.*

[6] *P. S. Brody, Investigation of Photovoltaic Ferroelectric Semiconductor Nonvolatile Memory, Harry Diamond Laboratories HDL-TR-1948 (March 1981).*

The charging is the result of the anomalous high-voltage photovoltaic ferroelectric ceramics. An open circuited photovoltaic ferroelectric ceramic element, when illuminated, will charge to a characteristic positive or negative voltage. The polarity of the charge depends on the direction of the electrically switchable remanent polarization. The magnitude of the voltage is proportional to the remanent polarization up to its maximum level. A capacitance placed across the element so as to shunt it will also be charged to that same saturation voltage level.

The characteristics of the switching are such that a two-state nonvolatile random access memory (RAM) is possible, operating with microsecond-duration write and erase pulses. In this report there are shown arrangements of cells and cell structures for such a device. Also discussed are approaches and problems in fabricating integrated devices.

New experimental work described in this report includes the performance of a test cell with respect to the various memory cell parameters. The test cell uses a sense transistor based on a junction field-effect transistor (JFET) rather than on the MOSFET device previously used.[5,6] There are also experiments in which the radiation hardness of the photovoltaic ferroelectric-semiconductor memory element was evaluated. These experiments indicate that the encoded polarization state and the photovoltaic mechanism are largely unaffected by both high total dose and dose rates of hard radiation.

2. JFET CELL AND TEST CIRCUIT

One arrangement has been described for a nonvolatile "sense transistor" cell element consisting of a ferroelectric element, two diodes, and a MOSFET.[5,6] Another functional equivalent using two JFET transistors and a photovoltaic ferroelectric element is shown schematically in figure 1. This new arrangement reduces by one the number of semiconductor components and also has advantages with respect to radiation hardness, since the more radiation-sensitive MOSFET has been eliminated as the sense transistor.

The functioning of this circuit is essentially the same as that of the MOSFET cell.[5,6] A positive voltage applied to the ferroelectric

---

[5] *P. S. Brody, Appl. Phys. Lett. 38 (February 1981), 673.*

[6] *P. S. Brody, Investigation of Photovoltaic Ferroelectric Semiconductor Nonvolatile Memory, Harry Diamond Laboratories HDL-TR-1948 (March 1981).*

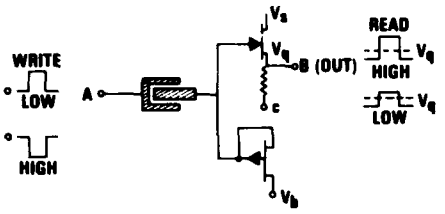


Figure 1. Arrangement using JFET transistors which makes dynamic cell sense transistor nonvolatile (not complete cell--write/read accessing elements are not shown).

element (which functions as a coupling capacitor) results in an instantaneous positive voltage at the gates, which then decays to a smaller positive voltage, V_s, plus the small drop across the diode through the n-channel JFET input diode during the write pulse duration, t_o. At time t_o the input of the capacitive element returns to ground, resulting in an instantaneous negative voltage at the gate, which decays rapidly to the negative voltage, V_b, less the diode drop through the p-JFET-based diode. The gate of the n-channel JFET (the sense transistor) is then charged to this negative voltage, which decays slowly through the high gate-to-ground resistance. This is the negative volatile gate memory charge.

A positive pulse applied to the ferroelectric element results, in a similar manner, in a positive volatile gate memory charge. The volatile memory states of the n-channel JFET sense transistor are controlled by these gate charges. A negative charge on the n-channel JFET gate from a positive write pulse increases the drain source channel resistance of the sense JFET, reducing the value of the quiescent voltage V_q, at B. If the transistor is operating near cutoff, this voltage, V_q, is small. The read output is then a low-level signal, indicating one of the binomial memory states, for example, a 0. A negative write pulse removes any negative gate charge, causing the channel resistance to decrease and increasing the quiescent voltage V_q to its high-level value, now indicating a 1. These read voltages are accessed with a read-access transistor (not shown). A column-select signal on the gate of the read-access transistor connects the sense transistor source point to a row. The row is accessed for read with a row-select signal at the gate of a row-access transistor.

The write pulses are applied with a transistor analog switch (not shown). The arrangement must be able to provide both positive and negative voltage pulses. In the tests described this is done with VMOS transistors, but more ideally a single JFET switch could be used. In that case the column and row address is produced by connecting the transistor drain to the desired positive or negative voltage source (column select) while simultaneously clamping the initially negative-biased gate to the source (row select).

The analog switches not only write by charging gates, but also switch the ferroelectric elements within the cells. When illuminated,

these elements charge the gate input capacitance to either a positive or negative voltage. The polarity of these voltages is the same as that of the volatile charge. If these voltages are equal to or greater than the gate voltage levels set by V_s and V_b, then the sense transistor returns to, or remains in, the last memory state addressed after the volatile charge vanishes. This provides the nonvolatile memory characteristics of the devices.

The test circuit (fig. 2) used ferroelectric memory elements which were bifilar planar electrode structures on a PZT-5A substrate. The memory elements were produced using a computer-generated reticle and negative photoresist. The substrates were 2-in.-diam, 0.015-in.-thick wafers of polished PZT-5A. Test element arrays (12 elements in an array) were formed 30 at a time on a single wafer. The wafer was then cut apart with a diamond blade. Each chip consisted of a single array. These were mounted in 14-pin dual in-line packages (DIP's), the terminals of which were connected to finger planar electrodes. Between a finger and a U-shaped central common electrode is a U-shaped gap across which the switching voltage will appear. Figure 3 is a photo-

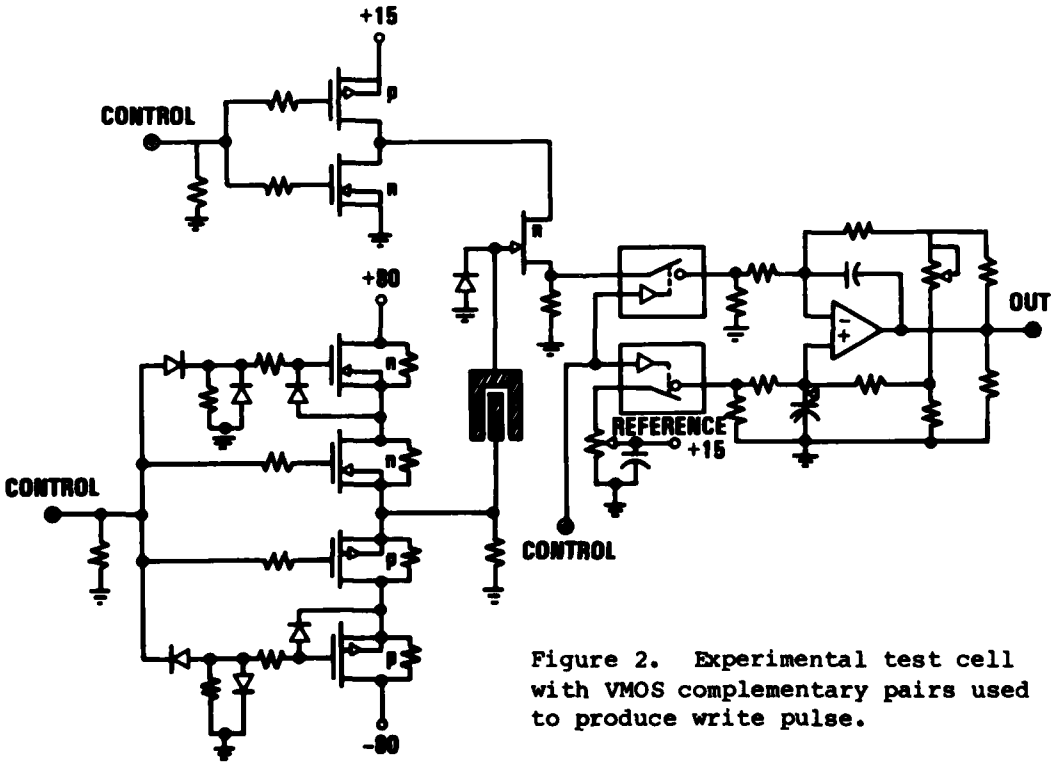


Figure 2. Experimental test cell with VMOS complementary pairs used to produce write pulse.

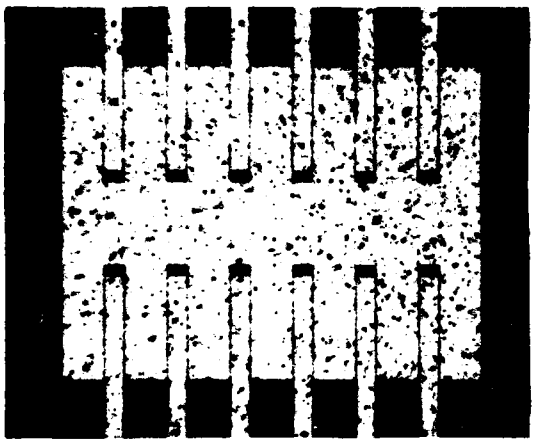


Figure 3. Photomicrograph of 12-element array. Metallization is Cr-Au.

micrograph of a 12-element array. The active regions that are the gaps are each 5 μm. The memory regions thus formed are 5000 μm^2 exclusive of electrodes. The fabrication yield was moderate with an occasional finger electrode in an array shorted to the common electrode.

For test purposes, an individual element--or memory region--is switched by connecting the element to the JFET gate and diode input and driving the common electrode positive or negative with a write pulse. For test purposes, an individual cell consisted of a single-array element in the test circuit shown.

2.1 Dependence of Read Outputs on Pulse Duration

An experimental test cell was constructed based on this new arrangement. The test circuit, shown in figure 2, was used to measure the dependence of the nonvolatile memory read outputs on write pulse duration. Plotted in figure 4 is the change in voltage at the source resistor measured 10 min after an encoding which reverses the element's spontaneous remanent polarization. During the 10-min interval, the initial volatile gate sense transistor gate charge has decayed. The charge on the gate is now the result of the photovoltaic output from the memory element. Illumination was from a 4-W fluorescent tube (GE F4T5 BLB) placed about 1 cm from the test DIP, producing about 1 mW/cm^2 of 370-nm centered radiation. The sense transistor circuit is a source follower. The change in output voltage is equal to the gate voltage change resulting from the photovoltaic charging, except for larger negative gate signals where the transistor cuts off. Figure 5 shows the dependence of the output voltage change on pulse voltage for a pulse duration of 300 ns. The effects of approaching saturation are seen, but saturation is not reached. The write voltages in these measurements were limited to ± 80 V by source gate breakdown in the V-groove MOS (VMOS) write circuits.

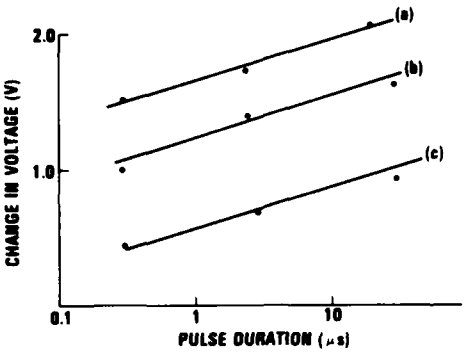


Figure 4. Quiescent voltage change as function of pulse duration for ± 74, ± 45, and ± 30 V switching pulses using test circuit in figure 2 and DIP array element.

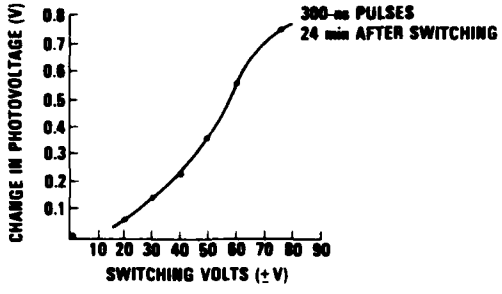


Figure 5. Dependence of gate photovoltage change on pulse magnitude.

2.2 Switching Characteristics

In a memory device it is preferable for the switching pulse to switch the ferroelectric polarization between two fully saturated states. Saturation will generally be difficult to achieve for low switching voltages and short pulse duration. The use of a double write pulse--a positive pulse followed by a negative pulse to produce the effect of a negative pulse (write high) and a negative pulse followed by a positive pulse to produce a single positive pulse (write low)--improves the situation for short duration write pulses. The double pulse system prevents the polarizations (and, therefore, the photoelectromotive forces--emf's) from walk-up and walk-down relative to a fixed level. The effectiveness of the double pulse method is a consequence of the hysterisis relation characteristic of polarity switching in the photovoltaic ferroelectric materials. Hysterisis relations between photovoltage and pulse number typical of the PZT-5A material are shown in figures 6 and 7. Note the softening of the loops for shorter duration pulses. In both cases, however, a reversing pulse is more effective in changing the element photovoltage than subsequent nonreversing pulses.

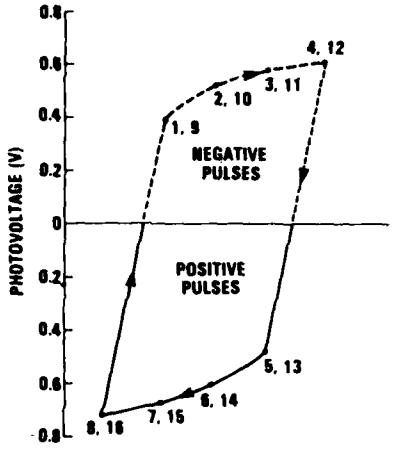


Figure 6. "Hysterisis" relation between photovoltage and number of pulses for 11-μs pulses.

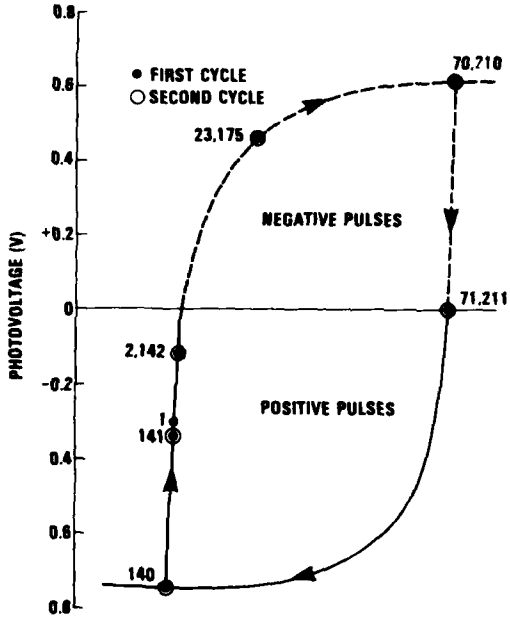


Figure 7. "Hysterisis" relation for 200-ns pulses.

In table 1 we see the results of experiments using asymmetric double pulses. Despite the varied sequences of read/write, the sense transistor output was always found to be in either a low voltage output (0.02 V) or a high voltage output (0.5 V) state. Two-state operation is clearly demonstrated. The tests also demonstrate at least 10^7 writes for arbitrarily varied sequences of high and low writes.

TABLE 1. EFFECT OF VARIED SEQUENCE OF WRITE-HIGH AND WRITE-LOW PULSES USING ASYMMETRIC POLARITY DOUBLE PULSE WRITES

Number of successive writes		Output after final write of series of successive writes (V)
1	Low	0.02
1	High	0.48
2×10^6	Low	0.02
1	High	0.48
1	Low	0.02
1	High	0.50
1×10^6	High	0.55
2×10^6	High	0.58
1	Low	0.07
1	High	0.44
1	Low	0.05
4×10^6	High	0.45
1	Low	0.02

Note: The experimental arrangement shown in figure 2 with a single memory element was used in these tests.

2.3 Retentivity of Stored Data

The decay of the photovoltage (which controls the memory state) with time is initially logarithmic and eventually levels off, supporting the expectation of indefinitely long memory retentivity.[5] Figure 8 shows memory retention results using the JFET test cell. A linear extrapolation of the plotted data shows the memory window closing in

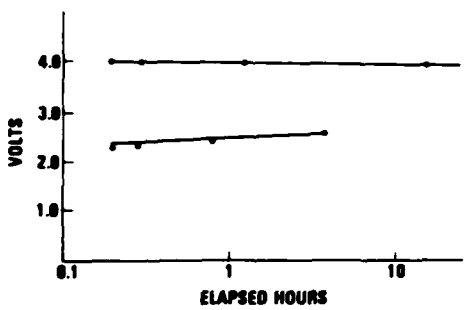


Figure 8. Memory photovoltage versus elapsed time for two memory states.

[5] *P. S. Brody, Appl. Phys. Lett. 38 (February 1981), 673.*

about 35 years. A linear extrapolation, however, is a worst possible assumption, since the logarithmic decay rate decreases with increasing time.

2.4 Radiation Hardness

The effects of total γ radiation dose on memory retention, and on the functioning of the ferroelectric element as a photovoltaic charge generator, were examined. An encoded single element mounted in a DIP element was subjected to an incrementally increasing total γ dose. The element was then returned to the test circuit. As before, a 4-W fluorescent tube was used as the illumination source. The results shown in figure 9 are photovoltages remeasured about 30 min after removing a test array element from a ^{60}Co source. For the higher total doses the initial photoelectromotive force was somewhat decreased from the initial value. The magnitude, however, increased with time over a period of several hours to the initial value. This temporary decrease is possibly due to a temporary darkening produced by the radiation. The darkening, however, vanished with time.

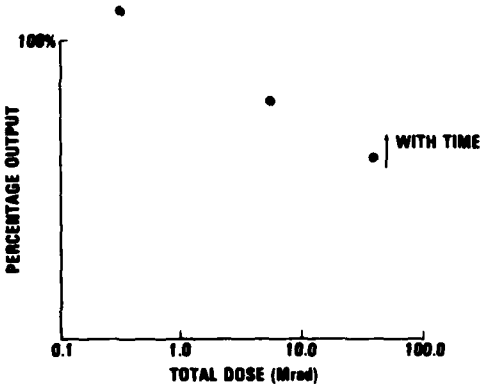


Figure 9. Results of total γ radiation dose on memory retention.

The effects of $\dot{\gamma}$ were determined by exposing a similar test array which had been encoded to a flash x-ray dose of 2×10^{11} rads/s. The device was then returned to the test fixture and read out. There was no significant change in sense transistor output.

These experiments show an intrinsic radiation hardness of the memory elements. The photovoltaic ferroelectric element is, however, just one portion of a memory cell. The remaining components are semiconductor elements--in particular, a sense transistor, which must continue to function normally after irradiation. This transistor, in MNOS and floating gate devices, is by necessity a very high impedance

device. The isolation of the floating gate charge, or of the interfacial MNOS charges retained in traps, is necessary in these devices. There must be no leakage of stored charge over the life of the memory state. This means that the conductivity of the insulating material isolating the gate (floating gate) from the channel must be very low. Radiation, however, has the effect of increasing conductivity, which reduces memory lifetime, and also creating charged defects, which can overwhelm the effects of the stored memory charge. MNOS and floating gate devices tend therefore to be radiation sensitive. The photovoltaic ferroelectric-semiconductor arrangement, however, can use a lower impedance sense transistor--e.g., a JFET used in the test device (see fig. 1 and 2), because there is a generation mechanism available for placing charges on the transistor gate. The energy for the charge generation comes from illumination incident on the photovoltaic element. The gate can be charged at any time during the indefinitely long life of the polarization state. An isolated packet of charge need therefore not be retained over the life of the memory, and the insulation between gate and channel need therefore not be as high as in floating gate or MNOS types. This semiconductor structure used with the ferroelectric element in a memory cell can therefore be of a type that is lower in impedance and is more radiation resistant. The photovoltaic semiconductor memory has, in this respect, an important advantage over the MNOS and floating gate charge retention memories.

3. APPLICATIONS TO RAM NONVOLATILE MEMORY--*CONTINUOUS ILLUMINATION*

The cell described in section 2 can be used with a continuous source of energizing illumination as a high-speed nonvolatile electronic RAM. The RAM application is interesting because there is no presently available device that would appear to be competitive with respect to permanence and speed. The continuous illumination form of the RAM memory has the two following characteristics:

(1) The transistor states persist, as addressed, even after the volatile gate charges have decayed. No overhead circuitry is needed to refresh the gates. The device is thus a static memory (although the cell structure is basically of the dynamic type) in the sense that refresh is not required.

(2) It is nonvolatile in the sense that if all power including illumination is removed, the information within the matrix is not lost. Restoring power and illumination returns each transistor or output to its correct value.

3.1 Application to Electrically Programmable and Electrically Alterable Read-Only Memory

A relatively simple scheme involves electrically addressing ferroelectric elements in matrix fashion in a programming device. Once programmed, the device is used as a read-only memory (ROM), but can be reprogrammed electrically very rapidly. Continuous or periodic pulse illumination provides the gate charges. A continuous illumination source keeps the gates charged or charges them when the memory is to be read out. The rate at which the gates charge and the total fluence (total optical energy in joules) required to charge the gates depend on the intensity and wavelength of the illumination and the gate-to-ground or channel capacitance and leakage. The gate-to-ground capacitance depends not only on the sense transistor capacitance to ground but also on the way the ferroelectric element is structured and the electrode configured. A lower limit on energy required to charge a gate to a specified voltage and a lower limit on illumination flux can, however, be obtained. The result of these calculations points to high densities and low optical energy fluence requirements in integrated devices.

The special requirements for an illumination source are compensated for by beneficial attributes of indefinitely long memory, retentivity, fast write times, and good environmental characteristics.

3.2 Nonvolatile RAM Requiring Illumination Only to Restore Memory States

A continuous source of illumination is not required for RAM. Illumination need be used only to restore lost memory states. To do this, cells are arranged in a matrix with refresh circuitry to operate as a dynamic RAM. If it were just an ordinary dynamic RAM, the memory data would be lost if the operating power were lost, or if the refresh cycle were interrupted (for another reason). In the photovoltaic ferroelectric semiconductor devices, however, the information stored at the time of the interruption is retained in the switchable ferroelectric elements. To restore normal operation after cycle interruption, the ferroelectric elements are all simultaneously illuminated with a low-level uv flood source. Figure 10 shows schematically the interrupt and restoration. Once the gates are recharged, the transistors will be in the correct memory states. Normal refresh can begin again and the illumination source removed.

This scheme is of the dynamic type. Refresh circuitry is required. A memory of the static type--but similar in other respects--can also be designed. As is true in a volatile static memory, a more complex cell structure would be necessary.

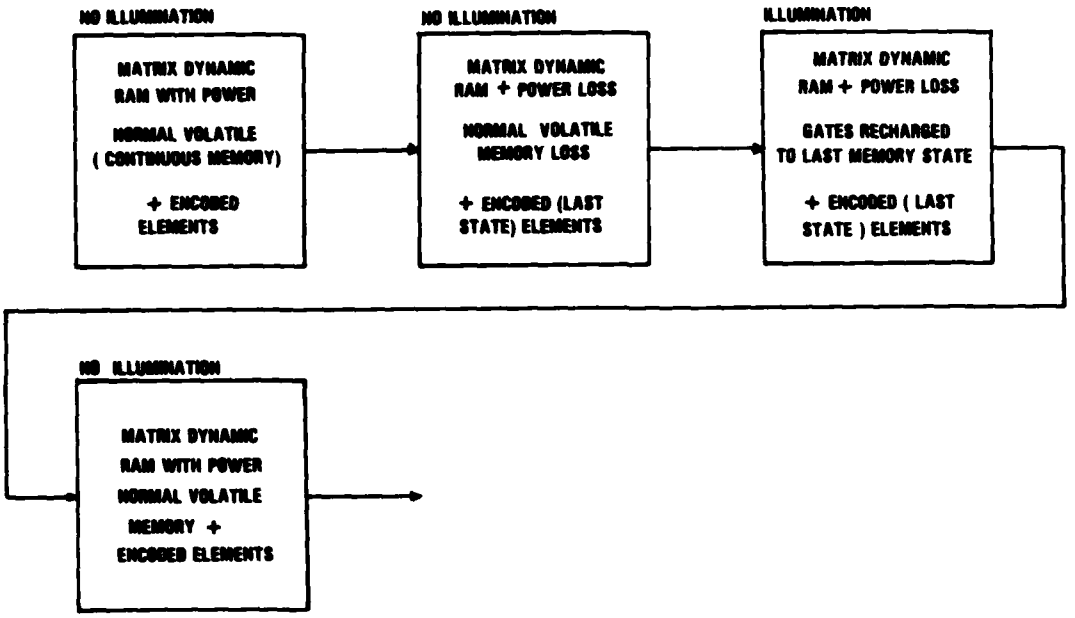


Figure 10 Scheme for nonvolatile photovoltaic ferroelectric-semiconductor RAM. To restore lost information, device is energized with low-level illumination flux.

4. APPROACH TO INTEGRATED DEVICES

Fully integrated devices could be fabricated with photovoltaic ferroelectric film memory elements on a silicon substrate. Integrated into the substrate would be a write transistor, a read access transistor, and a sense transistor with the photovoltaic ferroelectric memory elements as islands on the substrate. There are numerous possible cell configurations and element electrode configurations. In one configuration ferroelectric memory elements are arranged with edge electrodes or with planar electrodes, with the remanent polarization and photocurrent flow perpendicular to the direction of an illumination flux. This is called a transverse configuration in accordance with photoconductivity nomenclature. In another configuration--a so-called longitudinal configuration--the flux and polarization are parallel and the illumination passes through transparent electrodes. The transverse configuration was used for the experimental devices described in this report and in previous publications, but it is not necessarily the preferred arrangement.

The technology required for producing polycrystalline and single crystal films with ferrolectric properties on silicon and oxide substrates has been previously reviewed.[6] A typical process utilizes rf sputtering and subsequent thermal annealing. The annealing process converts the sputtered material, which is in an amorphous or a microcrystalline state, to a polycrystalline material with 0.1 μm or larger crystal grains.

For the configuration shown in figure 1, the switching and access transistors could be JFET or other MOS structures, or even bipolar devices. Either dielectric or junction isolation could be used for required isolations.

It is understood that in integrated devices switching voltages must be maintained within moderate limits. Voltages as high as those used in the experimental device require high voltage transistors, a capability which in the experimental devices is provided by the VMOS. It is felt, however, that element voltage requirements can be very considerably reduced--by reducing element size or by using ferroelectric materials with lower coercive fields. Even with the material used, PZT-5A switching voltages may be reduced to less than 10 V by increasing minimum write time to milliseconds (rather than microseconds).

In an integrated device, cell densities would be primarily controlled by the size of the semiconductor portion of the cells. The area requirements of the ferroelectric element islands would not be large. Based on known constants, one computes that a sense transistor with a 1-pF gate capacitance would be charged to its memory photovoltage in 1 s by a 5- by 100-μm edge-configured P2T-5A structure, using an illumination flux of 0.3 mW/cm^2. This is a density of 2×10^5 elements per cm^2 exclusive of requirements for spacing and connections.

5. CONCLUSIONS

The experimental analysis presented in this report supports the feasibility of moderate to high-density semiconductor EAPROM and RAM memory devices that use the photovoltaic effect in ferroelectric elements. The advantages over present devices exist in the potential for microsecond duration read/write cycle times, indefinitely long-time memory retentivity, and insensitivity of the intrinsic memory states to hard radiation. In addition, integrated devices can utilize JFET transistors which are less sensitive to hard radiation than the MOS structures used in floating gate devices.

---

[6] *P. S. Brody, Investigation of Photovoltaic Ferroelectric Semiconductor Nonvolatile Memory, Harry Diamond Laboratories HDL-TR-1948 (March 1981).*

There appears to be a potential for high density devices. One particularly attractive embodiment of the photovoltaic ferroelectric semiconductor memory concept would be a high density device which would function normally as an ordinary high-speed RAM with refresh circuitry. If the refresh cycle is lost--for example, by power shutoff--the memory states could be restored by a low-level illumination of the memory chips for several seconds.

LITERATURE CITED

(1) P. S. Brody, Solid State Comm. 12 (1973), 673.

(2) P. S. Brody, J. Solid State Chemistry 12 (1975) 673.

(3) For a recent review, see R. Von Baltz, Bulk Photovoltaic Effect in Ferro-and Piezoelectric Materials, Ferroelectrics, 35 (1981), 131.

(4) P. S. Brody, Ferroelectrics 38 (1981), 939.

(5) P. S. Brody, Appl. Phys. Lett. 38 (February 1981), 673.

(6) P. S. Brody, Investigation of Photovoltaic Ferroelectric Semiconductor Nonvolatile Memory, Harry Diamond Laboratories HDL-TR-1948 (March 1981).

DISTRIBUTION

ADMINISTRATOR
DEFENSE TECHNICAL INFORMATION CENTER
ATTN DTIC-DDA (12 COPIES)
CAMERON STATION, BUIDLING 5
ALEXANDRIA, VA 22314

COMMANDER
US ARMY RSCH & STD GP (EUR)
ATTN CHIEF, PHYSICS & MATH BRANCH
FPO NEW YORK 09510

COMMANDER
US ARMY ARMAMENT MATERIEL
READINESS COMMAND
ATTN DRSAR-LEP-L, TECHNICAL LIBRARY
ROCK ISLAND, IL 61299

DIRECTOR
US ARMY MATERIEL SYSTEMS ANALYSIS
ACTIVITY
ATTN DRXSY-MP
ABERDEEN PROVING GROUND, MD 21005

DIRECTOR
US ARMY BALLISTIC RESEARCH
LABORATORY
ATTN DRDAR-TSB-S (STINFO)
ABERDEEN PROVING GROUND, MD 21005

US ARMY ELECTRONICS TECHNOLOGY
& DEVICES LABORATORY
ATTN DELET-DD
ATTN DELET-IA-D, H. METTE
FT MONMOUTH, NJ 07703

DEPT OF DEFENSE
9800 SAVAGE ROAD
ATTN J. J. STRUNGE, EE
FT MEADE, MD 20755

ADVISORY GROUP ON ELECTRON DEVICES
201 VARICK STREET, 9TH FLOOR
ATTN WORKING GROUP B
NEW YORK, NY 10014

DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS
ATTN LIBRARY
ATTN K. GALLOWAY
WASHINGTON, DC 20230

DIRECTOR
DEFENSE ADVANCED RESEARCH
PROJECTS AGENCY
ARCHITECT BLDG
1400 WILSON BLVD
ATTN MATERIALS SCIENCES
ATTN ADVANCED CONCEPTS DIV
ATTN R. REYNOLDS
ARLINGTON, VA 22209

DIRECTOR
NATIONAL SECURITY AGENCY
ATTN S. LUBS
ATTN JOHN DAVIS
ATTN TECHNICAL LIBRARY
ATTN T. BROWN
ATTN P. DEBOY
ATTN G. DAILY
ATTN E. BUTALE (R-125)
FT MEADE, MD 20755

DIRECTOR
DEFENSE NUCLEAR AGENCY
ATTN TISI, SCI INFO DIV
ATTN TITL, TECH LIB DIV (4 COPIES)
ATTN RAEV, ELECTRONICS VUL DIV
ATTN RAEV, W. MOHR
ATTN RAEV, C. KIMBERLIN
WASHINGTON, DC 20305

UNDER SECRETARY OF DEFENSE
FOR RESEARCH & ENGINEERING
ATTN RESEARCH & ADVANCED TECH
WASHINGTON, DC 20301

ASSISTANT SECRETARY OF THE ARMY
RES, DEV, & ACQ
ATTN DEP FOR SCI & TECH
WASHINGTON, DC 20310

OFFICE OF THE DEPUTY CHIEF OF STAFF
FOR RESEARCH, DEVELOPMENT, & ACQ
ATTN DIR OF ARMY RES,
DR. M. E. LASSER
WASHINGTON, DC 20310

COMMANDER
US ARMY AVIONICS RES & DEV ACTIVITY
ATTN DAVAA-I, AVIATION ELECTRONICS
INTEGRATION DIV
ATTN DAVAA-E, COMMUNICATIONS &
SENSOR DIV
FT MONMOUTH, NJ 07703

DIRECTOR
BMD ADVANCED TECHNOLOGY CENTER
DEPARTMENT OF THE ARMY
PO BOX 1500
ATTN ATC-T
ATTN ATC-D
ATTN BMOSC-HW, R. DEKALB
HUNTSVILLE, AL 35807

DIRECTOR
ELECTRONICS TECHNOLOGY &
DEVICES LABORATORY
US ARMY ERADCOM
ATTN DELET-DT, DIR TECHNICAL PLANS &
PROGRAMS OFFICE

ELECTRONICS TECHNOLOGY &
DEVICES LABORATORY (Cont'd)
ATTN DELET-E, DIR ELECTRONIC
MATERIALS RESEARCH DIV
ATTN DELET-I, DIR MICROELECTRONICS
DIV
FT MONMOUTH, NJ 07703

DIRECTOR
ELECTRONIC WARFARE LABORATORY
ATTN DELEW-SM, EW SYSTEMS MGT OFFICE
ATTN DELEW-E, ELCT INTEL/CM DIV
ATTN DELEW-V, EM VULN & ACCM DIV
FT MONMOUTH, NJ 07703

DIRECTOR
US ARMY MISSILE LABORATORY
USAMICOM
ATTN DRSMI-RPR, REDSTONE SCIENTIFIC
INFO CENTER
REDSTONE ARSENAL, AL 35809

DIRECTOR
NIGHT VISION & ELECTRO-OPTICS
LABORATORY
ATTN DELNV-AC, ADVANCED CONCEPTS DIV
ATTN DELNV-IRT, INFRARRED TECH DIV
ATTN DELNV-L, LASER DIVISION
ATTN DELNV-R, ELECTRO-OPTICS RES
ATTN DELNV-SI, OPTICS
ATTN DELNV-SI, ELECTRONICS
ATTN DELNV-VI, VISIONIC DIVISION
FT BELVOIR, VA 22060

ARMY RESEARCH OFFICE (DURHAM)
PO BOX 12211
ATTN DRXRO-EL, DIR ELECTRONICS DIV
ATTN DRXRO-PH, DIR PHYSICS DIV
ATTN DRXRO-MS, METALLURGY-MATERIALS
DIV
ATTN DRXRO-EG, DIR ENGINEERING DIV
RESEARCH TRIANGLE PARK, NC 27709

DIRECTOR
US ARMY SIGNALS WARFARE LABORATORY
VINT HILL FARMS STATION
ATTN DELSW-CE, COMMUNICATIONS/EW DIV
ATTN DELSW-EE, ELECTRONICS/EW DIV
ATTN DELSW-OS, OFFICE OF
THE SCIENTIFIC ADVISOR
WARRENTON, VA 22186

DIRECTOR
NAVAL RESEARCH LABORATORY
ATTN 2600, TECHNICAL INFO DIV
ATTN 2750, OPTICAL SCIENCES DIV
ATTN 6000, MATL & RADIATION
SCI & TE
ATTN CODE 5347, J. ALTER, EE
ATTN CODE 5216, H. HUGHES
ATTN CODE 6816, D, PATTERSON
WASHINGTON, DC 20375

CHIEF OF NAVAL RESEARCH
DEPT OF THE NAVY
ATTN ONR-420, PHYSICAL SCI DIV
ATTN CODE 427, L. COOPER
ARLINGTON, VA 22217

COMMANDER
NAVAL SURFACE WEAPONS CENTER
ATTN DX-21 LIBRARY DIV
DAHLGREN, VA 22448

COMMANDER
NAVAL SURFACE WEAPONS CENTER
ATTN F30, NUCLEAR EFFECTS DIV
ATTN R-42, ELECTRO-OPTICS BR
ATTN X-22, TECHNICAL LIB
ATTN CODE F31
WHITE OAK, MD 20910

AIR FORCE WRIGHT AERONAUTICAL LAB
ATTN DHE, J. GARRETT
ATTN DHE, F. SCHUERMEIER
ATTN DEH, C. YOUNG
WRIGHT-PATTERSON AFB, OH 45433

COMMANDER
HQ ROME AIR DEVELOPMENT CENTER
(AFSC)
ATTN LE, DEPUTY FOR ELECTRONIC TECH
GRIFFISS AFB, NY 13441

AF WEAPONS LABORATORY, DYC
ATTN EL, ELECTRONICS DIV
ATTN LR, LASER DEV DIV
ATTN ELP, J. MULLIS
ATTN ELP, R. TALLON
KIRTLAND AFB, NM 87117

DIRECTOR
NASA
LANGLEY RESEARCH CENTER
ATTN TECHNICAL LIBRARY
ATTN PAUL HAYES, FLIGHT EQUIPMENT
DIV, MAILSTOP 470 (25 COPIES)
ATTN A. FRIPP
HAMPTON, VA 23665

RADC/RBRP
ATTN C. LANE
GRIFFISS AFB, NY 13441

RADC/ESR
ATTN P. J. VAIL
ATTN SHEDD
ATTN B. BUCHANAN
HANSCOM AFB, MA 01731

DISTRIBUTION (Cont'd)

SANDIA NATIONAL LABORATORIES
PO BOX 5800
ATTN R. K. TREECE, STF MBR
ATTN D. S. HILL, MTS, DIV 4734
ATTN J. THOMAS CUTCHEN
ATTN G. R. LAGUNA
ATTN C. E. LAND
ATTN J. K. G. PANITZ
ATTN W. A. WENRICH, DIV 1761
ATTN T. A. DELLIN
ATTN R. JONES
ALBUQUERQUE, NM 87185

SANDIA NATIONAL LAB
ATTN R. GREGORY
ATTN P. DRESSENDORFER
ATTN J. JORGENSEN
ATTN W. DAWES
ATTN M. KNOLL
ATTN W. DODSON
ATTN H. STEIN
ALBUQUERQUE, NM 87115

ADVANCED MICRO DEVICES
902 THOMPSON PLACE
ATTN Y. J. WANG, ENGR
ATTN J. SCHLAGETER
SUNNYVALE, CA 94086

ADVANCED RSCH & APPLICATIONS CORP
ATTN L. PALCUTTI
1223 E. ARQUES AVENUE
SUNNYVALE, CA 94086

AEROJET ELECTRO-SYSTEMS CO
ATTN D. TOOMB
PO BOX 296
AZUSA, CA 91702

AMD INC
23064 EVERGREEN LANE
ATTN R. BOWER
LOS GATOS, CA

AMD
ATTN SAL CAGNINA
ATTN DARRELL RINERSON
M/S 37
901 THOMPSON PLACE
SUNNYVALE, CA 94086

AMDAHL CORP
1250 E. ARQUES
ATTN J. FOGGIATE, PRO MGR
ATTN L. JUBB
SUNNYVALE, CA 94086

AMI
ATTN R. BROZE
3800 HOMESTEAD RD
SANTA CLARA, CA 95051

APPLIED MATERIALS, INC
3050 BOWERS AVE
ATTN W. C. BENZING
SANTA CLARA, CA 95051

JOHNS HOPKINS APPLIED PHYSICS LAB
JOHNS HOPKINS ROAD
ATTN J. WENIG
ATTN S. D. COX
ATTN G. D. WAGNER
ATTN P. PARTRIDGE
LAUREL, MD 20810

APPLIED RES LABS EAD
PO BOX 8029
ATTN K. BUTLER
AUSTIN, TX 78712

APPLIED MICROSYSTEMS
11064 118TH PLACE NE
ATTN L. E. LINDBLOOM, MKT MGR
KIRTLAND, WA 98033

BELL TELEPHONE LABORATORIES
600 MOUNTAIN AVE
ATTN T. NEGRAN
ATTN A. M. GLASS
ATTN H. M. O'BRYAN
ATTN J. M. GEARY
ATTN P. C. MICHAELIS, MTS
MURRAY HILL, NJ 07974

CALIFORNIA INSTITUTE OF TECHNOLOGY
JET PROPULSION
ATTN M. BEUHLER
4800 OAK GROVE DR.
PASADENA, CA 91103

CHARLES STARK DRAPPER LAB INC
ATTN R. BEDINGFIELD
ATTN TECH LIB
ATTN A. RENARD
ATTN K. SMITH
ATTN J. KRONICK
ATTN A. MARQUIS
555 TECHNOLOGY SQUARE
CAMBRIDGE, MA 02139

CONTROL DATA CORP
ATTN T. FRYE
PO BOX O
MINNEAPOLIS, MN 55440

DASTEK CORP
141 ALBRIGHT WAY
ATTN A. GINDI, MGR
LOS GATSO, CA 95030

DATA ACQUISITION
3799 SOUTH 2235 E
ATTN E. G. YOUNG, ENGR
SALT LAKE, UT 84109

DATA GENERAL MS D216
4400 COMPUTER DRIVE
ATTN L. THIBEAULT
ATTN S. GEROGIS
WESTBORO, MA 01580

DATA GENERAL CORP
BOX 297
ATTN R. MOLNAR
EASTFORD, CT 06242

DATA PRODUCTS CORP
6219 DE SOTO AVE
ATTN Y WONG, ENGR
WOODLAND HILLS, CA 91365

DEC
301 ROCKRIMMON BLVD S
ATTN M. A. BROWN, SEN ENGR
COLO SPGS, CO 80919

DIGITAL EQUIP CORP
1925 & OVER ST
ATTN J. SOFIC
ATTN H. E. KEMPTON
TEWKSBURY, MA 01876

DIGITAL EQUIP CORP
506 BENNETT ST
ATTN A. C. MARTEL, SR ENG
GREENVILLE, SC 29609

ELECTRONICS INDUSTRIES ASSOC
2001 EYE STREET, NW
ATTN J. HESSMAN
WASHINGTON, DC 20006

ELECTRONIC MEMORIES &
MAGNETICS CORPORATION
ATTN T. C. TAYLOR
1600 VENTURA BLVD
ENCINO, CA 91430

EMM CORP
ATTN F. KRCH
3883 N 28TH AVE
PHOENIX, AZ 85017

EOCOM CORP
15771 REDHILL AVENUE
ATTN R. PRICHARD
TUSTIN, CA 92680

E SYSTEMS
PO BOX 1056
ATTN D. J. POUNDS
ATTN K. REIS
GREENVILLE, TX 75401

FAIRCHILD-ADVANCED R&D
ATTN ROGER T. BAKER
ATTN NING HSIEH
ATTN CHING JENG
ATTN DR. A. TICKL
4001 MIRANDA AVE
PALO ALTO, CA 94303

FAIRCHILD
ATTN YUKUN HSIA
3420 CENTRAL EXPRESSWAY
SANTA CLARA, CA 95051

GULTON INDUSTIRES, INC.
ATTN JOSEPH P. DOUGHERTY
METUCHEN, NJ 08840

HARRIS SEMICONDUCTOR
BOX 883
ATTN D. R. WILLIAMS
ATTN J. CORNELL
ATTN T. SANDERS
ATTN C. ANDERSON
ATTN J. BUXO
ATTN K. A. RODDE
ATTN B. K. ROSIER
MELBOURNE, FL 32901

HARRIS SEMICONDUCTOR
ATTN KEN PORTS
PROGRAMS DIV
PO BOX 883 M/S 51-121
PALM BAY, FL 32901

HEWLETT-PACKARD CO
ATTN H. WEGENER
ATTN TECH LIBRARY
ATTN T. W. EKSTEDT
3500 DEER CREEK ROAD
PALO ALTO, CA 94304

HONEYWELL
2600 RIDGWAY PKWY
ATTN S. CALLAGHAN
ATTN R. GUNN
MINNEAPOLIS, MN 55413

DISTRIBUTION (Cont'd)

HONEYWELL
2 FORBES RD
ATTN D. LEES, ENG
LEXINGTON, MA 02173

HONEYWELL CERAMICS CENTER
ATTN JOSEPH KOYONKA
GOLDEN VALLEY, MN 55422

HONEYWELL CORPORATE MATERIAL
SCIENCE CENTER
10701 LYNDALE AVE
ATTN S. T. LIU
ATTN S. LIE
BLOOMINGTON, MN 55420

HONEYWELL INC
AVIONICS DIVISION
ATTN R. WIKER
PO BOX 11563
ST PETERSBURG, FL 33733

HONEYWELL INC
SEMICONDUCTOR DIVISION
ATTN F. HAMPDEN
PLYMOUTH, MN 55400

HONEYWELL SSED
ATTN F. HAMPTON
1200 STATE HIGHWAY 55 M213-3016
PLYMOUTH, MN 55441

HUGHES AIRCRAFT
BOX 3310
ATTN J. M. KIRSCH, MTS
FULLERTON, CA 92633

HUGHES AIRCRAFT CO
PO BOX 6852
ATTN G. SHREVE, MTS
TORRANCE, CA 90504

HUGHES AIRCRAFT
EL SEGUNDO SITE
ATTN D. SCHUMAKE
ATTN E. SMITH
PO BOX 92919
LOS ANGELES, CA 90009

HUGHES AIRCRAFT CO.
ATTN P. BOHAC JR.
(700/A2234)
ATTN F. BOHAC
ATTN N. MOYER
ATTN B. PAYNTER
ATTN K. SHELTON
500 SUPERIOR AVE
NEWPORT BEACH, CA 92663

HUGHES AIRCRAFT CO
ATTN M. COLLIGAN
ATTN R. MCGOWAN
CENTINELA & TEALE
CULVER CITY, CA 90230

IBM
OLD ORCHARD ROAD
ATTN K. M. TRAMPEL, PTA MGR
ATTN B. HOWARD
ARMONK, NY 10504

IBM
18100 FREDERICK PK
ATTN D. A. RICHARD, ENGR
GAITHERSBURG, MD 20760

IBM
740 NEW CIRCLE RD
ATTN R. M. WOOTON, ENG
LEXINGTON, KY 40511

IBM
HWY 52N 2F8
ATTN A. GOLDSTEIN
ROCHESTER, MN 55901

IBM
1001 HARRIS BLVD
ATTN H. R. LEWIS, ENGR
ATTN GEOFF STEPHENS
CHARLOTTE, NC 28257

IBM CORP
5600 COTTLE RD
ATTN F. S. WIEDMER, SR ENGR
SAN JOSE, CA 95193

IBM
DEPT G9L B610 2
ATTN H. ROSS, ADV ENG
ATTN DR. FERRIS PRABHU
ESSEX JCT, VT 05452

IBM
ATTN CHUNG H. LAM
ATTN RONALD TROUTMAN
RIVER ROAD
ESSEX JUNCTION, VT 05452

IBM
BOV A M50 972 2
ATTN C. J. DANIELSKI, ADV ENG
ESSEX JCT, VT 05452

IBM
ATTN YU-NIAN HSIEH
NEIGHBOORHOOD RD
KINGSTON, NY 12401

IBM
ATTN D. J. DIMARIA
T. J. WATSO RESEARCH CTR
PO BOX 218
YORKTOWN HEIGHTS, NY 01598

IBM COMMUNICATION PRODUCT DIV
ATTN C. HOFFMAN
RALEIGH, NC 27611

IBM CORP
ATTN F. TIETSE
ROUTE 17C
OWEGO, NY 13827

IMP
ATTN MOIZ KHAMBATY
ATTN JAYASIMHA PRASAD
2830 N FIRST ST
SAN JOSE, CA 95134

INTEL CORP
3065 BOWERS AVE
ATTN A. STIVER, ENGR
ATTN J. MAR (MS 1-133)
ATTN W. JOHNSON
ATTN V. DHAM
ATTN B. EITAN
ATTN B. SHINER
ATTN M. HOLLER
ATTN M. VANBUSKIRK
ATTN M. WOODS
ATTN A. KOLODNY
ATTN CHENG-FONG JOSEPH JOU
ATTN J. LEE
ATTN J. MCCREARY
ATTN S. NIEH
ATTN R. PASHLEY
SANTA CLARA, CA 95051

INTERNATIONAL TEL & TELEGRAPH CORP
ATTN A. RICHARDSON
500 WASHINGTON AVE
NUTLEY, NJ 07110

IIT RESEARCH INSTITUTE
ATTN I. MINDEL
10 W 35TH STREET
CHICAGO, IL 60616

INTL TEL & TEL DCD
492 RIVER RD
ATTN J. CARMODY, MTS
NUTLEY, NJ 07110

INTERSIL INC
3250 SCOTT BLVD
ATTN D. MACDONALD
SANTA CLARA, CA 80906

INMOS CORP
ATTN G. DERVENWICK
2860 S CIRCLE DR
COLORADO SPRINGS, CO 80906

INMOS
ATTN G. DERBENWICK
ATTN A. LANCASTER
ATTN R. SOKEL
ATTN J. R. ADAMS
PO BOX 16000
COLORADO SPRINGS, CO 80935

INMOS CORP
ATTN R. JOHNSTONE
PO BOX 6900
COLORADO SPRINGS, CO 80935

INSTITUTE FOR DEFENSE ANALYSIS
ATTN TECH INFO SERVICES
400 ARMY-NAVY DRIVE
ARLINGTON, VA 22202

JET PROPULSION LAB
ATTN J. A. WURZBACK
ATTN F. GRUNTHANER
ATTN J. MASERJIAN
4800 OAK GROVE DR
PASADENA, CA 91103

LITTON
5500 CANOGA
ATTN J. R. HUDDLE
ATTN J. RETZLER
ATTN DR. H. C. ABBINK
WOODLAND HILLS, CA 91364

LITTON SYS
8000 WOODLEY AVE
ATTN S. J. STERNBACH
ATTN J. A. KLACKA, MGR
VAN NUYS, CA 91409

MCDONNELL DOUGLAS ASTRO
5301 BOLSA MS22 3
ATTN A. SOLOMON
ATTN Y. EDEN, ENG
ATTN D. FITZGERALD
ATTN G. KATE
HUNTINGTON BCH, CA 92647

QUESTRON CORP
ATTN D. WEBER
101 CONTINENTAL BLVD
SUITE 500
EL SEGUNDO, CA 90245

DISTRIBUTION (Cont'd)

QWIP SYS
1125 DUNCAN DR
ATTN T. D. LAPP
MAITLAND, FL 32751

QUANTEX CORP
252 N WOLDE ROAD
ATTN S. MALLICK, ENG
SUNNYVALE, CA 94086

RAMTEK
2211 LAWSON LN
ATTN S. J. RAICHLEN, DES ENG
SANTA CLARA, CA 95050

RAND CORP
ATTN C. CRAIN
1700 MAIN ST
SANTA MONICA, CA 90460

RAYTHEON
528 BOSTON POST RD
ATTN E. REILLY, ENGR
ATTN M. SEAVEY
ATTN H. FLESCHER
ATTN N. CAMPBELL
ATTN A. VANDOREN
SUDBURY, MA 01776

RCA CORP-GOVT SYSTEMS DIV
ASTRO ELECTRONICS
ATTN V. MANCINO
ATTN R. ANGLE
ATTN L. NAPOLI
PO BOX 800 LOCUST CORNER
PRINCETON, NJ 08540

RCA CORP
DAVID SARNOFF RSCH CTR
ATTN D. O'CONNOR
ATTN G. J. BRUCKER
PO BOX 432
PRINCETON, NJ 08540

RCA
ATTN R. G. STEWART
SW 106
PRINCETON, NJ 05840

RCA CORP
SOMERVILLE PLANT
SOLID STATE DIV
ATTN D. GLICKSMAN
SOMERVILLE, NJ 08876

SIGNETICS CORP
ATTN A. BHATTACHARYYA
ATTN P. KESHTBOD
811 E ARQUES AVE, MS 0502
SUNNYVALE, CA 94086

SPERRY FLIGHT SYS
21111 N 19TH AVE
ATTN E ELLIS, PROJ ENGR
ATTN R. NALETTE, PR ENGR
ATTN M. LEWIS, ENG 109B
ATTN D. SCHOW
PHOENIX, AZ 85036

SPERRY RAND CORP
SPERRY DIVISION
ATTN D. MARAFFINO
MARCUS AVE
GREAT NECK, NY 11020

SPERRY UNIVAC
ATTN J. INDA
ATTN M. A. HORNE
UNIVAC PARK
PO BOX 3525
ST PAUL, MN 55165

SYLVANIA SYSTEMS GROUP
ELECTRONICS SYS & SVC ORG
ATTN J. WALDRON
GTE PRODUCTS CORP
189 B ST
NEEDHAM, MA 02194

TELEDYNE MICROELECTRONICS
ATTN L. SUTTON
12964 PANAMA ST
LOS ANGELES, CA 90066

TEXAS INSTRUMENTS CORP
ATTN. W. CHAN (MS631)
ATTN G. ARMSTRONG
PO BOX 1443
HOUSTON, TX 77001

TEXAS INSTRUMENTS
PO BOX 1444
ATTN W. C. HUBBELL
ATTN B. ASHMORE, DSGNER
ATTN S. C. TSAUR, SE ENGR
ATTN J. L. PETERSON
HOUSTON, TX 77001

TEXAS INSTRUMENTS INC
PO BOX 226080
ATTN D. PINKOS, DES ENG
DALLAS, TX 75266

VERNITRON CORP
ATTN B. JAFFE
BEDFORD, OH 44146

WESTINGHOUSE
ATTN T. H. BEDRAREK
ATTN W. S. CORAK
ATTN A. EDWARDS

DISTRIBUTION (Cont'd)

WESTINGHOUSE (Cont'd)
ATTN P. C. SMITH
ATTN DR. P. R. SUTHERLAND
ATTN H. A. R. WEGENER
ATTN J. BREWER (M53525)
ATTN J. FAGAN
PO BOX 1521 M/S 3527
BALTIMORE, MD 21203

WESTINGHOUSE ELECTRIC CO
AEROSPACE & ELECTRONICS SYS DIV
ATTN ART EDWARDS
ATTN R. CRICCHI
PO BOX 1693
BALTIMORE-WASHINGTON INTL AIRPORT
BALTIMORE, MD 20203

WESTINGHOUSE RESEARCH LABORATORIES
ATTN JIM S. Y WU
PITTSBURGH, PA 15235

XEROX MEMORY SYSTEMS
3333 BOWERS AVENUE
ATTN P. M. BURTON
SANTA CLARA, CA 95051

US ARMY ELECTRONICS RESEARCH
& DEVELOPMENT COMMAND
ATTN TECHNICAL DIRECTOR, DRDEL-CT

HARRY DIAMOND LABORATORIES
ATTN CO/TD/TSO/DIVISION DIRECTORS
ATTN RECORD COPY, 81200
ATTN HDL LIBRARY, 81100 (2 COPIES)
ATTN HDL LIBRARY, 81100 (WOODBRIDGE)
ATTN TECHNICAL REPORTS BRANCH, 81300
ATTN CHAIRMAN, EDITORIAL COMMITTEE
ATTN LEGAL OFFICE, 97000
ATTN N. KARAYIANIS, 13200
ATTN G. SZTANKAY, 13300
ATTN B. DOBRIANSKY, 13500
ATTN A. EDWARDS, 13500
ATTN N. BERG, 15200
ATTN R. JOHNSON, 15200
ATTN E. BROWN, 00211
ATTN F. CROWNE, 13200
ATTN E. KATZEN, 13200
ATTN H. DROPKIN, 13200
ATTN R. LEAVITT, 13200
ATTN C. MORRISON, 13200
ATTN G. SIMONIS, 13200
ATTN M. TOBIN, 13200
ATTN D. WORTMAN, 13200
ATTN J. SATTLER, 13200
ATTN T. L. WORCHESKY, 13200
ATTN I. MARCUS, 48000
ATTN J. MCGARRITY, 22300
ATTN P. WINKOUR, 22300
ATTN J. HALPIN, 22800
ATTN F. W. BAKLICKI 20240
ATTN P. BRODY, 13200 (100 COPIES)


ME
83